Low Power Integrated Circuit Design Using Compressed Sensing and Dictionary Learning

PhD Proposal Seminar by
Jie (Jack) Zhang
Graduate Research Assistant (Dr. Ralph Etienne-Cummings)
Electrical and Computer Engineering

Abstract
In the signal processing domain, the theory of Compressed Sensing (CS) indicates that a sparse signal can be represented using fewer samples compared to its Nyquist rate. This discovery has shed new light on the community since the Shannon-Nyquist era. Since its introduction, CS has been applied to many applications such as designing ADC for high speed RF signals, reducing MRI scanning time and designing low power pixel sensors consisting of only a single photodiode. By combining CS with Dictionary Learning, a technique for constructing a scarifying dictionary, new clustering and classification methods are also invented for face-recognition, object detection and classification.

In this proposal, I will discuss two projects where new circuits and systems are built inspired by the theory of CS and Dictionary Learning to improve system efficiency. In the first project (CS-NEURAL), I outline a low power neural recording device targeted to reduce chip power consumption by >90% while guaranteeing signal reconstruction quality. In the second project (CS-IMAGER), I propose a fast and power efficient CMOS image sensor for mobile wireless sensor node (MWSN) that can sample a fast scene using low frame with low motion blurring. I will also demonstrate preliminary chip testing results in 180nm CMOS process.

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FOR DISABILITY INFORMATION CONTACT: Janel Johnson (410) 516-7031 janel.johnson@jhu.edu